TMC22071A

Genlocking Video Digitizer

Features

- Fully integrated acquisition
- 3-channel video input multiplexer
- Two-stage video clamp
- Automatic gain adjustment
- Sync detection and separation
- Pixel and subpixel adjustment of HSYNC-to-Video timing
- Genlock to NTSC or PAL inputs
- Clock generation
- 8-bit video A/D converter
- Microprocessor interface
- Line-locked pixel rates
  - 12.27 MHz NTSC
  - 13.5 MHz NTSC or PAL
- Direct interface to TMC22x9x encoders
- Built-in circuitry for crystal oscillator
- No tuning or external voltage reference required
- 68 Lead PLCC or 100 Lead MQFP package

Applications

- Frame grabber
- Digital VCR/VTR
- Desktop video

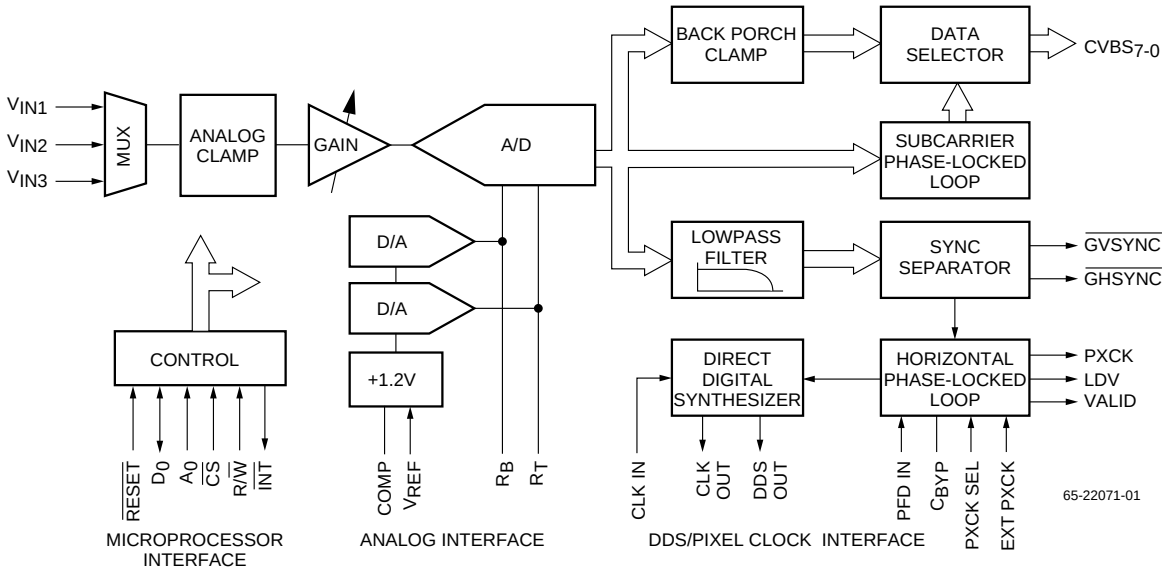
Description

The TMC22071A Genlocking Video Digitizer converts standard baseband composite NTSC or PAL video into 8-bit digital composite video data. It extracts horizontal and vertical sync signals and generates a pixel clock for the on-board 8-bit A/D converter and a 2x clock for the transfer of data to subsequent video processing decoding or encoding with the TMC22x5y Video Decoder or TMC22x9x Digital Video Encoder family. It also measures the color subcarrier phase and frequency and provides this data to the Encoder (for genlocked color NTSC or PAL encoding), or a frame buffer (for frame capture) over the digital composite video port.

The TMC22071A includes a three-channel video input multiplexer, analog clamp, variable gain amplifier, and digital back porch clamp. The on-board oscillator circuitry generates the clock from a 20 MHz crystal or the clock source may be an external oscillator. It is programmable over a microprocessor interface for NTSC or PAL operation. No external component changes and no production tuning or service adjustments are ever required.

The TMC22071A is fabricated in an advanced CMOS process, and is packaged in a 68 Lead PLCC or 100 Lead MQFP. Its performance is guaranteed from 0°C to 70°C.

Block Diagram



Functional Description

The TMC22071A is a fully-integrated genlocking video A/D converter which digitizes NTSC or PAL baseband composite video under program control. It accepts video on three selectable input channels, adjusts gain, clamps to the back porch, and digitizes the video at a multiple of the horizontal line frequency. It extracts horizontal and vertical sync, measures the subcarrier frequency and phase (relative to the sampling clock), and provides the data along with digital composite video data over an 8-bit digital video port. Two sync outputs ($\overline{\text{GHSYNC}}$ and $\overline{\text{GVSYNC}}$) are also provided. It generates 1x (LDV) and 2x (PXCK) pixel clocks for data transfer. PXCK also serves as a master clock for the companion TMC22x9x Encoders and TMC22x5y decoders.

Operating parameters are set up via a serial microprocessor port. Internal or external voltage reference operation is available

Timing

The TMC22071A operates from an internally-synthesized clock, PXCK, which runs at twice the pixel data rate. The nominal pixel rates may be set to 12.27 Mpps for NTSC and 13.5 Mpps for NTSC and PAL. Customers requiring 14.75 or 15 Mpps PAL operation should consult factory.

Video Input

Three high-impedance video inputs are selected by an internal multiplexer under host processor control. The device accepts industry-standard video levels of 1.23 Volts (sync tip to peak color = 1 volt sync tip to reference white). Good channel-to-channel isolation allows active video on all three inputs simultaneously. Antialiasing filtering (if used) and line termination resistors must be provided externally. The input selection is controlled by two bits in the Control Register.

Analog Clamp

The front-end analog clamp ensures that the input video falls within the active range of the A/D converter. The digitized composite video output can be clamped to the back porch by a secondary digital clamp.

Automatic Gain Adjustment

Since video signals may vary substantially from nominal levels, the TMC22071A performs an automatic level setting routine to establish correct signal amplitudes for digitizing.

The TMC22071A relies upon the presence of the sync tip-to-back porch voltage to determine the gain required for the input video signal.

Sync tip compression or clipping is often affected by APL (Average Picture Level) variation. Rather than tracking minor variations in sync tip amplitude and constantly adjusting video gain, the TMC22071A establishes proper signal amplitudes during initial genlock acquisition, and then (optionally) holds the gain constant. This results in a stable picture under variable signal conditions.

Improperly terminated or weak video signals are handled in the TMC22071A by a selectable gain of +1.0 or +1.5. The higher gain can amplify a doubly-terminated signal which is reduced in amplitude by 2/3.

If the input signal levels are well controlled, the automatic gain adjustment can be disabled and the gain held at its nominal value (unity or 1.5X).

Analog-to-Digital Converter

The TMC22071A contains a high-performance 8-bit A/D converter. Its gain and offset are automatically set as a part of the automatic gain adjustment process during initial signal acquisition, and require no user attention.

The reference voltages to the A/D converter are set up by internal D/A converters under automatic control during genlock acquisition. These voltages determine the gain and offset of the A/D converter with respect to the video level presented at its input.

Low-Pass Filter

The digitized composite video stream is digitally low-pass filtered to remove chrominance components from the sync separator. Filtering provides robust operation by optimizing the signal-to-noise ratio of the synchronizing/blanking portion of the video, improving the accuracy of the back porch blanking level detector.

A digital sync separator provides the output sync signals, $\overline{\text{GHSYNC}}$ and $\overline{\text{GVSYNC}}$, and times internal operations.

Horizontal Phase-Locked Loop

A phase-locked loop generates PXCK, at twice the pixel rate. The reference signal for the horizontal phase-locked loop is generated by the Direct Digital Synthesizer (DDS). The DDS output is constructed with an internal D/A converter and is output from the TMC22071A via the DDS OUT pin. This signal is passed through an external LC filter and input to the horizontal phase-comparator.

The frequency of the DDS output is one ninth of that of PXCK.

A 20 MHz clock is required to drive the DDS. Preferably, this may be input to the TMC22071A via CMOS levels on the CLK IN pin. Alternately, a 20 MHz crystal may be directly connected between CLK IN and $\overline{\text{CLK}}$ OUT with tuning capacitors to activate the internal crystal oscillator circuitry.

If incoming video is lost or disconnected after the TMC22071A has acquired and locked, PXCK, $\overline{\text{GHSYNC}}$,

$\overline{\text{GVSYNC}}$ and GRS data will continue. The GRS data will be the initial subcarrier frequency and phase values selected by the Format select bits of the Control Register. The TMC22071A will acquire and lock to incoming video within two frames after video is restored.

Subcarrier Phase-Locked Loop

A fully-digital phase-locked loop is used to extract the phase and frequency of the incoming color burst. These frequency and phase values are output over the CVBS bus during the horizontal sync period. Fairchild's video decoder and genlockable encoder chips will accept these data directly.

Back Porch Digital Clamp

A digital back-porch clamp is employed to ensure a constant blanking level. It digitally offsets the data from the A/D converter to set the back porch level to precisely $3C_h$ for NTSC and 40_h for PAL. When the digital clamp is enabled, the CVBS video output data is determined from the A/D conversion result minus the back porch level + $3C_h$ (40_h for PAL).

Digitized Video Output

The digitized 8-bit video output is provided over an 8-bit wide CVBS data port, synchronous with PXCK and LDV. Subcarrier frequency, subcarrier phase, and Field ID data (GRS) are transmitted in 4-bit nibbles over $CVBS_{3-0}$ during the horizontal sync tip period at the PXCK rate.

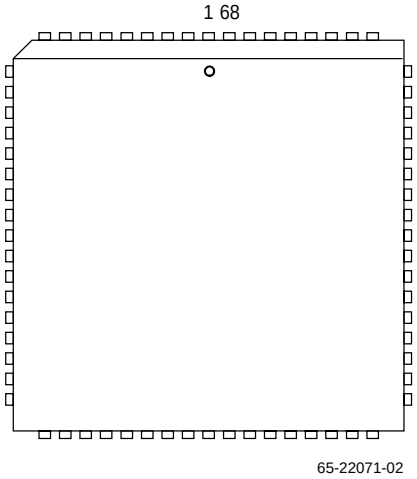
Microprocessor Interface

Since microprocessor buses are notoriously noisy from a wide-band analog point of view, the microprocessor interface bus is only one bit wide, rather than the more customary eight. The operation of this bus is similar to other bus-controlled devices except that the TMC22071A internal Control Register is accessed one bit at a time.

A sequence of 47 bits is written to or read from the LSB of a standard microprocessor port. Writing to or reading from the secondary address results in the transfer of data to or from the internal shift register.

The $\overline{\text{RESET}}$ input, when LOW, sets all internal state machines to their initialized conditions. Returning the $\overline{\text{RESET}}$ pin HIGH starts the signal acquisition sequence which lasts until locking with the gain-adjusted and clamped video signal is achieved.

Pin Assignments



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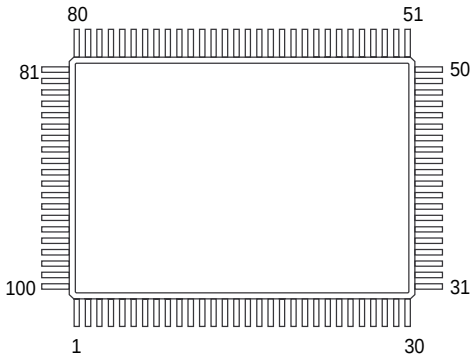
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	18	V_{DD}	35	A_{GND}	52	V_{DD}
2	$CVBS_0$	19	PXCK	36	R_T	53	$\overline{\text{CLK}}$ OUT
3	$CVBS_1$	20	D_{GND}	37	A_{GND}	54	EXT PXCK
4	$CVBS_2$	21	D_{GND}	38	V_{REF}	55	D_{GND}
5	$CVBS_3$	22	V_{DD}	39	A_{GND}	56	D_{GND}
6	$CVBS_4$	23	V_{DDA}	40	V_{DDA}	57	D_{GND}
7	V_{DD}	24	A_{GND}	41	A_{GND}	58	V_{DD}
8	D_{GND}	25	V_{DDA}	42	C_{BYP}	59	V_{DD}
9	$CVBS_5$	26	V_{DDA}	43	PFD IN	60	A_0
10	$CVBS_6$	27	A_{GND}	44	A_{GND}	61	R/$\overline{\text{W}}$
11	$CVBS_7$	28	R_B	45	DDS OUT	62	$\overline{\text{CS}}$
12	$\overline{\text{GHSYNC}}$	29	V_{IN3}	46	PXCK SEL	63	V_{DD}
13	$\overline{\text{GVSYNC}}$	30	V_{DDA}	47	V_{DDA}	64	$\overline{\text{RESET}}$
14	VALID	31	V_{IN2}	48	COMP	65	D_{GND}
15	D_{GND}	32	A_{GND}	49	A_{GND}	66	D_0
16	D_{GND}	33	V_{DDA}	50	D_{GND}	67	$\overline{\text{INT}}$
17	LDV	34	V_{IN1}	51	CLK IN	68	D_{GND}

Pin Assignments (continued)



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	A_0	26	V_{DD}	51	V_{DDA}	76	NC
2	NC	27	D_{GND}	52	V_{DDA}	77	PFD IN
3	NC	28	$CVBS_5$	53	NC	78	NC
4	R/$\overline{W}$	29	$CVBS_6$	54	NC	79	NC
5	$\overline{CS}$	30	$CVBS_7$	55	A_{GND}	80	NC
6	V_{DD}	31	NC	56	NC	81	A_{GND}
7	$\overline{RESET}$	32	$\overline{GHSYNC}$	57	R_B	82	DDS OUT
8	D_{GND}	33	$\overline{GVSYNC}$	58	V_{IN3}	83	NC
9	D_0	34	VALID	59	NC	84	NC
10	NC	35	NC	60	V_{DDA}	85	NC
11	NC	36	NC	61	V_{IN2}	86	PXCK SEL
12	NC	37	NC	62	NC	87	V_{DDA}
13	NC	38	D_{GND}	63	A_{GND}	88	COMP
14	NC	39	D_{GND}	64	V_{DDA}	89	A_{GND}
15	NC	40	LDV	65	V_{IN1}	90	D_{GND}
16*	D_{GND}	41*	D_{GND}	66	NC	91	CLK IN
17	$\overline{INT}$	42*	V_{DD}	67	A_{GND}	92	V_{DD}
18	V_{DD}	43	NC	68	R_T	93	$\overline{CLK}$ OUT
19	NC	44	V_{DD}	69	A_{GND}	94	EXT PXCK
20	NC	45	PXCK	70	V_{REF}	95	D_{GND}
21	$CVBS_0$	46	D_{GND}	71	NC	96	D_{GND}
22	$CVBS_1$	47	D_{GND}	72	A_{GND}	97	D_{GND}
23	$CVBS_2$	48	V_{DD}	73	V_{DDA}	98	V_{DD}
24	$CVBS_3$	49	V_{DDA}	74	A_{GND}	99	NC
25	$CVBS_4$	50	A_{GND}	75	C_{BYP}	100	V_{DD}

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Notes:

1. NC = Do Not Connect.
* These pins are not connected in the TMC22071A. However, you should connect these pins as shown for compatibility with future genlock ICs.

Pin Definitions

Pin Name	Pin Number 68 pin PLCC	Pin Number 100 pin MQFP	Pin Type	Function
Video Input				
V_{IN1-3}	34, 31, 29	65, 61, 58	1.23Vp-p	**Composite Video Input.** Video inputs,1.25 Volts peak-to-peak, sync tip to peak color
Clocks				
CLK IN	51	91	CMOS	**20 MHz DDS clock input.** 20 MHz CMOS clock input to DDS. This pin may also be used along with $\overline{CLK}$ OUT for directly connecting crystals.
$\overline{CLK}$ OUT	53	93	CMOS	**Inverted clock output.** Inverted DDS clock output. This pin may also be used along with CLK IN for directly connecting a crystal.
PXCK	19	45	CMOS	**2x Pixel clock output.** 2x oversampled line-locked clock output.
LDV	17	40	CMOS	**Pixel clock output.** Delayed pixel clock output. LDV runs at 1/2 the rate of PXCK and its rising edge is useful for transferring CVBS digital video from the TMC22071A to the TMC22x9x Digital Video Encoders.
EXT PXCK	54	94	CMOS	**External PXCK input.** Input for external PXCK clock source.
PXCK SEL	46	86	CMOS	**PXCK source select.** Select input for internal or external PXCK. When HIGH, the internally generated line-locked PXCK is selected. When LOW, the external PXCK source is enabled.

Pin Definitions (continued)

Pin Name	Pin Number		Pin Type	Function
	68 pin PLCC	100 pin MQFP		
Digital Video				
$\overline{GHSYNC}$	12	32	CMOS	**Horizontal sync output.** When the TMC22071A is locked to incoming video, the $\overline{GHSYNC}$ pin provides a negative-going pulse after the falling edge of the horizontal sync pulse. There is a fixed number of PXCK clock cycles between adjacent falling edges of $\overline{GHSYNC}$, except following a VCR headswitch.
$\overline{GVSYNC}$	13	33	CMOS	**Vertical sync output.** When the TMC22071A is locked to incoming video, the $\overline{GVSYNC}$ pin provides a negative-going edge after the start of the first vertical sync pulse of a vertical blanking interval.
$CVBS_{7-0}$	11-9, 6-2	30-28, 25-21	CMOS	**Composite output bus.** 8-bit composite video data is output on this bus at 1/2 the PXCK rate. During horizontal sync, field ID, subcarrier frequency, and subcarrier phase are available on this bus.
µP I/O				
D_0	66	9	TTL	**Data I/O port.** Microprocessor data port. All control parameters are loaded into and read back from the Control Register over this 1-bit bus.
A_0	60	1	TTL	**µP port control.** Microprocessor address bus. A LOW on this input loads the I/O Port Shift Register with data from D_0 and $\overline{CS}$. A HIGH transfers the I/O Port Shift Register contents into the Control Register on the last falling edge of $\overline{CS}$.
$\overline{CS}$	62	5	TTL	**Chip select.** When $\overline{CS}$ is HIGH, D_0 is in a high-impedance state and ignored. When $\overline{CS}$ is LOW, the microprocessor can read or write D_0 data into the Control Register.
$\overline{RESET}$	64	7	TTL	**Master reset input.** Bringing $\overline{RESET}$ LOW forces the internal state machines to their starting states, loads the Control Register with default values, and disables outputs. Bringing $\overline{RESET}$ HIGH restarts the TMC22071A in its default mode.
R/$\overline{W}$	61	4	TTL	**Bus read/write control.** When R/$\overline{W}$ and A_0 are LOW, the microprocessor can write to the Control Register over D_0. When R/$\overline{W}$ is HIGH and A_0 is LOW, the contents of the Status Register are read over D_0.
$\overline{INT}$	67	17	TTL	**Interrupt output.** This output is LOW if the internal horizontal phase lock loop is unlocked with respect to incoming video for 128 or more lines per field. After lock is established, $\overline{INT}$ goes HIGH.
VALID	14	34	TTL	**HSYNC locked flag.** This output, when HIGH indicates that incoming horizontal sync has been detected within the ±16 pixel window in time established by previous sync pulses. When LOW, it indicates that incoming horizontal sync has not been found within the expected time frame. VALID will toggle if the time stability of incoming video is such that sync positioning varies more than ±16 pixels or if occasional horizontal sync pulses are missing.

Pin Definitions (continued)

Pin Name	Pin Number 68 pin PLCC	Pin Number 100 pin MQFP	Pin Type	Function
Analog Interface				
V_{REF}	38	70	+1.23 V	**V_{REF} input/output.** +1.23 Volt reference. When the internal voltage reference is used, this pin should be decoupled to A_{GND} with a 0.1 μF capacitor. An external +1.2 Volt reference may be connected here, overriding the internal reference source.
COMP	48	88	0.1 μF	**Compensation capacitor.** Compensation for DDS D/A converter circuitry. This pin should be decoupled to V_{DDA} with a 0.1 μF capacitor.
R_T,R_B	36, 28	68	0.1 μF	**A/D V_{REF} decoupling.** Decoupling points for A/D converter voltage references. These pins should be decoupled to A_{GND} with a 0.1 μF capacitor.
PLL Filter				
DDS OUT	45	82		**Internal DDS output.** Analog output from the internal Direct Digital Synthesizer D/A converter, at 1/9 the PXCK frequency.
PFD IN	43	77		**Horizontal PLL input.** Analog input to the Phase/Frequency Detector of the horizontal phase-locked loop.
C_{BYP}	42	75	1 μF	**Comparator bypass.** Decoupling point for the internal comparator reference of the Phase/Frequency Detector. This pin should be decoupled to A_{GND} with a 0.1 μF capacitor.
Power Supply				
V_{DDA}	23, 25, 26, 30, 33, 40, 47	49, 51, 52, 60, 64, 73, 87	+5 V	**Analog power supply.** Positive power supply to analog section.
V_{DD}	1, 7,18, 22, 52, 58,59,63	6, 18, 26, 42, 44, 48, 92, 98, 100	+5 V	**Digital power supply.** Positive power supply to digital section.
Ground				
A_{GND}	24, 27, 32, 35, 37, 39, 41, 44, 49,	50, 55, 63, 67, 69, 72, 74, 81, 89	0.0 V	**Analog ground.** Ground for analog section.
D_{GND}	8, 15, 16, 20, 21, 50, 55-57, 65, 68	8, 16, 27, 38, 39, 41, 46, 47, 90, 95-97	0.0 V	**Digital ground.** Ground for digital section.

Control and Status Registers

The TMC22071A is controlled by a single 47-bit long Control Register. Access to the Control Register is via the I/O Port Shift Register arranged as shown in Figure 1. The Control Register can be written, with the desired programming. The 12-bit Status Register is read-only and accessed through the same l/O Port Shift Register. Reading the Status Register yields information about blanking level, subcarrier presence, and whether or not PXCK is locked or unlocked with respect to the line rate.

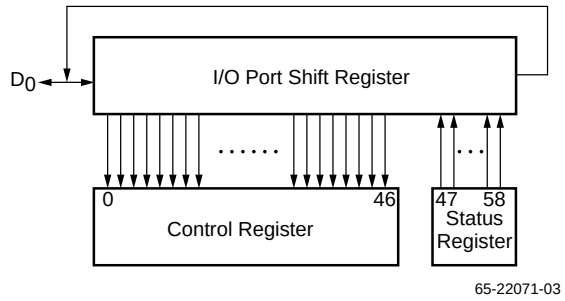


Figure 1. Control and Shift Register Structure

The host processor writes data into the TMC22071A using only one bit of the microprocessor's data and address bus. As shown in Figure 2, the user should bring A_0 high for the $\overline{CS}$ falling edge preceding the introduction of bit 0 to the D_0 port. The next rising edge of $\overline{CS}$ completes the preloading of the control data, which transfer into the control register on the next rising edge of the pixel clock. The I/O Port Shift Register, Control Register and Status Register are governed by $\overline{CS}$, R/$\overline{W}$, and A_0. R/$\overline{W}$ and A_0 are latched by the TMC22071A on the falling edge of $\overline{CS}$ and data input D_0 is latched on the rising edge of $\overline{CS}$. Data read from D_0 is enabled by the falling edge of $\overline{CS}$ and disabled by the rising edge of $\overline{CS}$. When the Control Register is read more than once consecutively, an extra $\overline{CS}$ pulse and accompanying A_0 is needed to align the circulated shift register data.

Table 1. Microprocessor Port Control

A_0	R/$\overline{W}$	Action
0	0	Write data from D_0 into l/O Port Shift Register
0	1	Read D_0 data from last stage of l/O Port Shift Register
1	0	Transfer l/O Port Shift Register contents to Control Register
1	1	Enables continuous update of status bits in l/O Port Shift Register

The full sequence of 47 bits of Control Register data must be written each time a change in that data is desired. All or a few of the Control and Status Register bits may be read, but the sequence always begins with bit 58 of the Status Register.

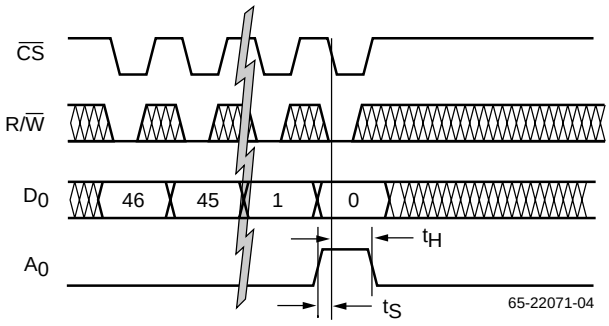


Figure 2. Data Write Sequence

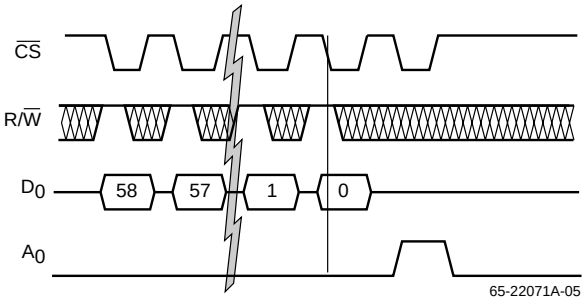


Figure 3. Data Read Sequence

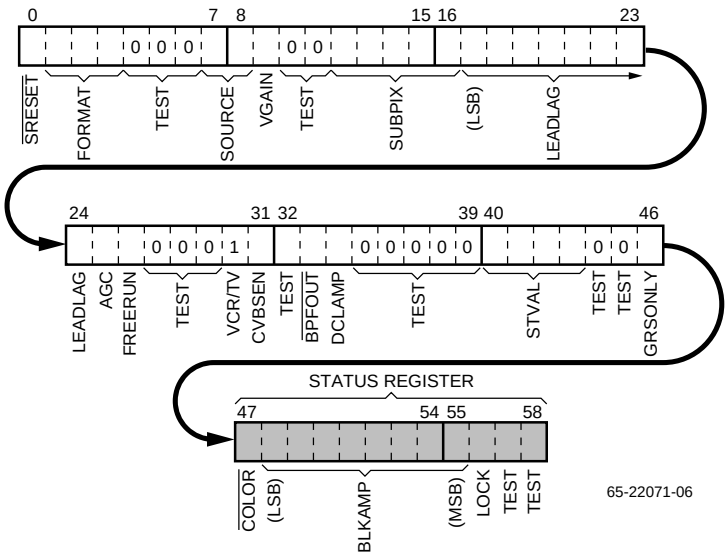


Figure 4. Control Register Map

Control Register Bit Functions

Bit	Name	Function
0	SRESET	Software reset. When LOW, resets and holds internal state machines, resets Control Register with previously written values, and disables output drivers. When HIGH, SRESET starts and runs state machines, PXCK, and enables outputs.
1-3	FORMAT	Input signal format select. Bit 3 is the MSB. 000 NTSC at 12.27 Mpps. 001 NTSC at 13.5 Mpps. 010 Reserved. 011 Reserved. 100 PAL at 13.5 Mpps. 101 Reserved. 11x Reserved.
4-6	TEST	Factory test control bits. These should be set LOW.
7,8	SOURCE	Video source select. Bit 8 is the MSB. 00 V_{IN1} 01 V_{IN2} 1x V_{IN3}
9	VGAIN	Video gain. When LOW, gain is set to unity. When HIGH, gain is set to 1.5X.
10-11	TEST	Factory test control bits. These should be set LOW.
12-16	SUBPIX	These control bits allows the HSYNC, VSYNC, and sample clock to be time-shifted by -16/32 to +15/32 pixels. Bit 16 is the two's complement MSB. When SUBPIX is 00_h, HSYNC and incoming video are subject to LEADLAG. A value of 18_h delays HSYNC 1/4 pixel. A value of 08_h advances HSYNC 1/4 pixel.
17-24	LEADLAG	This control word allows the HSYNC and VSYNC to be time-shifted -122 to +132 LDV cycles. When LEADLAG is $7B_h$, HSYNC and incoming video are in alignment. A value of 83_h delays HSYNC eight LDV cycles. A value of 73_h advances HSYNC eight LDV cycles. Bit 24 is the MSB.

Control Register Bit Functions (continued)

Bit	Name	Function
25	AGC	AGC operation control. After H and V sync acquisition, the A/D converter references are adjusted to encompass the full video range. The system can initiate an A/D adjustment sequence at any time by bringing this bit HIGH. The control bit will reset to 0 following AGC adjustment.
26	FRERUN	When HIGH, a free-running PXCK is generated, independent of incoming video. When LOW, PXCK is locked to incoming video.
27-29	TEST	Factory test control bits. These should be set LOW.
30	VCR/TV	Block sync enable. When HIGH the TMC22071A accepts both normal and block sync. (In block sync, the incoming signal is at the sync tip level for 2.5 (PAL) or 3 (NTSC) consecutive lines. Equalization pulses may be absent.) When LOW, only normal sync may be input. For most applications, whether using a VCR or a studio video input source, best performance will be found when this bit is HIGH.
31	CVBSEN	CVBS bus enable. When LOW, the $CVBS_{7-0}$, $\overline{GHSYNC}$, and $\overline{GVSYNC}$ outputs are in a high-impedance state. When HIGH, they are enabled.
32	TEST	Factory test control bit. This should be set LOW.
33	$\overline{BPFOUT}$	Burst phase / frequency output control. When HIGH, GRS is disabled. When LOW, burst phase and frequency information is output on $CVBS_{3-0}$.
34	DCLAMP	Digital clamp enable. The digital clamp is enabled when DCLAMP is HIGH and disabled when LOW.
35-39	TEST	Factory test control bits. These should be set LOW.
40-43	STVAL	Sync tip value. When DCLAMP is HIGH and STVAL is set to its default value 3_h the output sync level is 3_h for NTSC and 7_h for PAL. Bit 43 is the MSB.
44	$\overline{VCR}$	VCR lock control. Setting this bit LOW improves the TMC22071A's locking to VCR signals. When only clean video input signals are used, the user may set this bit HIGH for compatibility with existing TMC22071 firmware.
45	TEST	Factory test control bit. This should be set LOW.
46	GRSONLY	When the horizontal phase lock loop becomes unlocked (i.e. after video input is disconnected) and this Control Bit is HIGH, all CVBS data is forced LOW except subcarrier frequency and phase data (GRS). $\overline{GHSYNC}$, $\overline{GVSYNC}$, and PXCK continue with default GRS data until video is required. The presence of GRS also depends upon bit 33. If the GRSONLY bit is LOW, $\overline{GHSYNC}$, $\overline{GVSYNC}$, and PXCK continue with default GRS data continue but video pixel data is random.
Status Bits (Read Only)		
47	COLOR	Burst present status bit. This bit is HIGH when burst is present on the input video. It is LOW, when burst is not present.
48-55	BLKAMP	Blanking amplitude status bit. These eight bits report the actual blanking level.
56	$\overline{LOCK}$	H-lock loop status bit. When HIGH, the TMC22071A is not locked to an input signal. When LOW, lock has been achieved.
57-58	TEST	These are read-only bits for testing puposes only.

Horizontal Timing

Horizontal line rate is selectable, and is determined by the FORMAT control bits (12.27 Mpps for NTSC, 13.5 Mpps for NTSC and PAL). Figure 5 illustrates the horizontal blanking interval. Figure 6 completes the definition of timing parameters with vertical blanking interval detail.

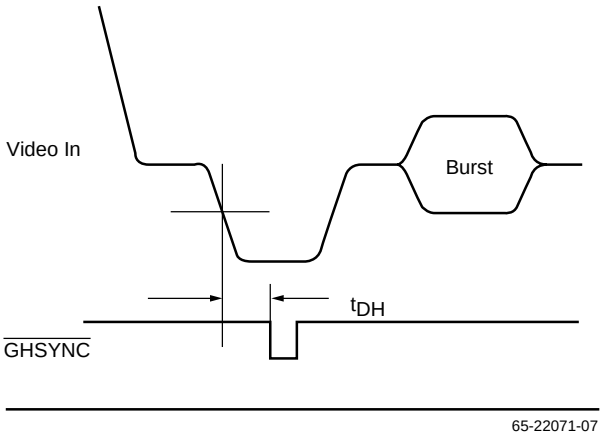


Figure 5. Horizontal Sync Timing

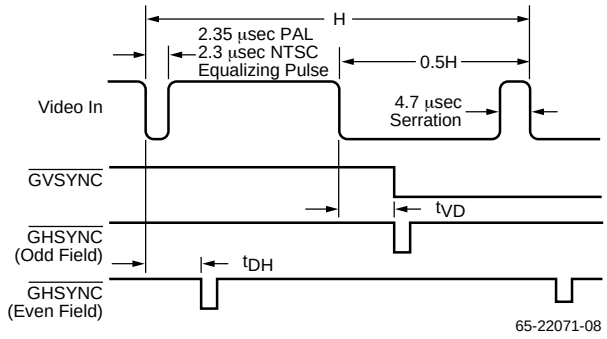


Figure 6. Vertical Sync timing

Programming the TMC22071A

Upon power-up after bringing $\overline{\text{RESET}}$ LOW, the TMC22071A Control Register is set to default values as shown in the top entry of Table 3. These default values do not necessarily render the TMC22071A operational in any specific application. Before the TMC22071A is expected to acquire input video, its Control Register must be loaded with data that is specific to its use.

Table 2.TMC22071A Timing Options

Standard	Field Rate (Hz)	Line Rate (kHz)	Pixel Rate (Mpps)	PXCK Frequency (MHz)	Plxels Per Line
NTSC	59.94	15.734264	12.2727+	24.54+	780
NTSC-601	59.94	15.734264	13.50	27.0	858
PAL-601	50.00	15.625	13.50	27.0	864

Table 3. Control Register Example Data

	Control Register Data (Bit 56 …… Bit 0)											
Standard	46	42	38	34	30	26	22	18	14	10	6	2
DEFAULT	0000	0110	0000	1001	0000	0010	0000	0000	0000	0000	0000	001
NTSC	0010	0110	0000	1001	1000	0010	0000	0000	0000	00xx	0000	000
NTSC-601	0010	0110	0000	1001	1000	0010	0000	0000	0000	00xx	0000	010
PAL-601	0010	1110	0000	1001	1000	0010	0000	0000	0000	00xx	0001	xx0

CVBS Bus Data Formats

The CVBS bus outputs a Genlock Reference Signal (GRS) along with the 8-bit digital composite video data. The range of output data versus video input voltage is illustrated in Figure 7 where sync tip and blanking levels are controlled by the digital backporch clamp of the TMC22071A. During horizontal sync, the TMC22071A outputs field identification, subcarrier frequency, and subcarrier phase information on the CVBS bus.

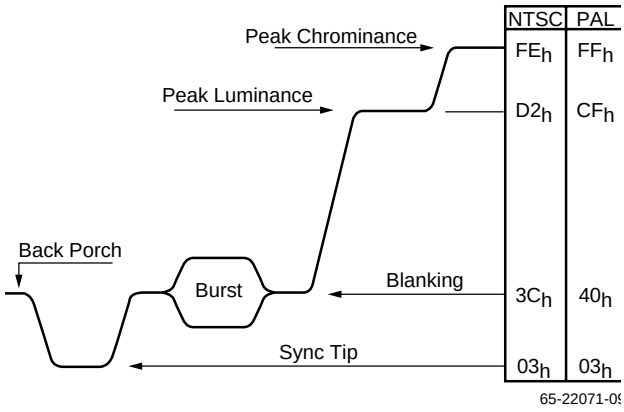


Figure 7. Output Data vs. Input Video Level

Field identification is output on $CVBS_{2-0}$. The LSB, $CVBS_0$, will be LOW during odd fields and HIGH for even fields. When NTSC operation is selected, $CVBS_{1-0}$ count 00,01,10,11 for fields 1 through 4 respectively. When PAL operation is selected, $CVBS_{2-0}$ count 000, 001, 010, etc. to 111 for fields 1 through 8, respectively.

$CVBS_3$ indicates V-component inversion in PAL. It is HIGH for NTSC lines (burst 135°) and LOW for PAL lines (burst 225°)

Subcarrier frequency is sent out in a 24-bit binary representation in six 4-bit nibbles on $CVBS_{3-0}$. Subcarrier frequency data, f_{23-0}, is identical to the pre-programmed BSEED value used in the TMC22071A to lock the subcarrier phase-locked loop to the incoming subcarrier frequency.

Subcarrier phase, Φ_{23-0}, is also sent out in a 24-bit binary representation in six 4-bit nibbles on $CVBS_{3-0}$. Bit Φ_{23} is the MSB.

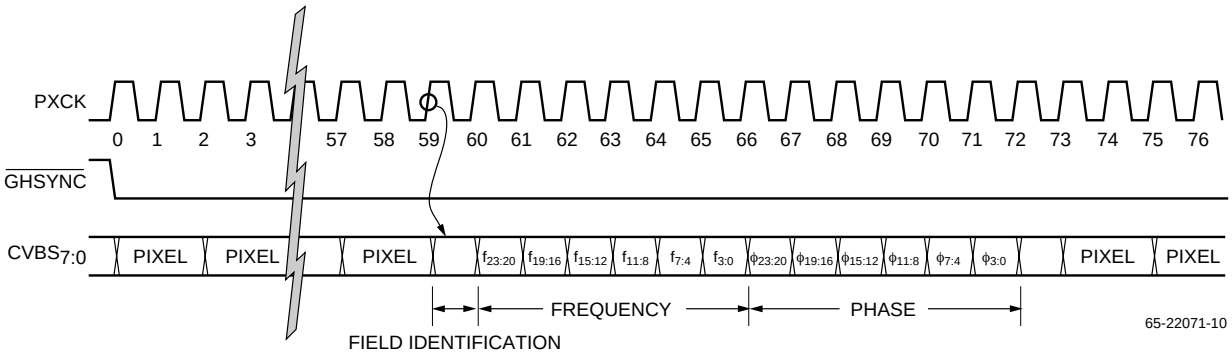


Figure 8. Genlock Reference Signal (GRS) Format

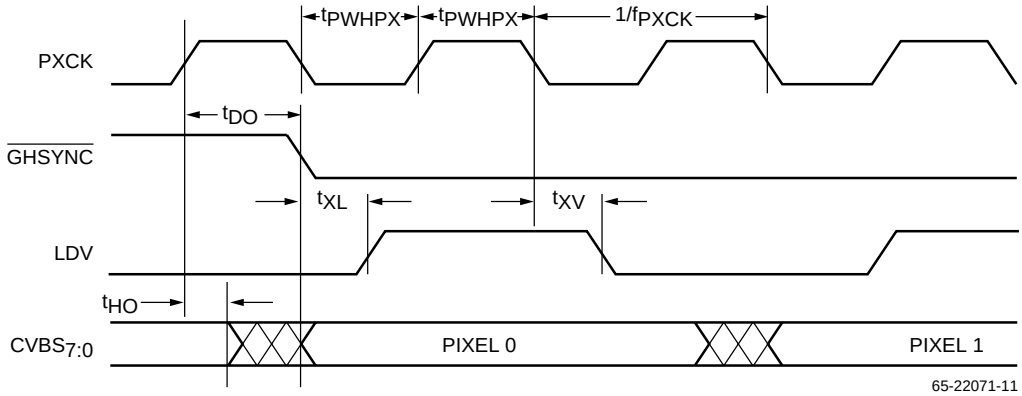


Figure 9. CVBS Bus Video Data Format

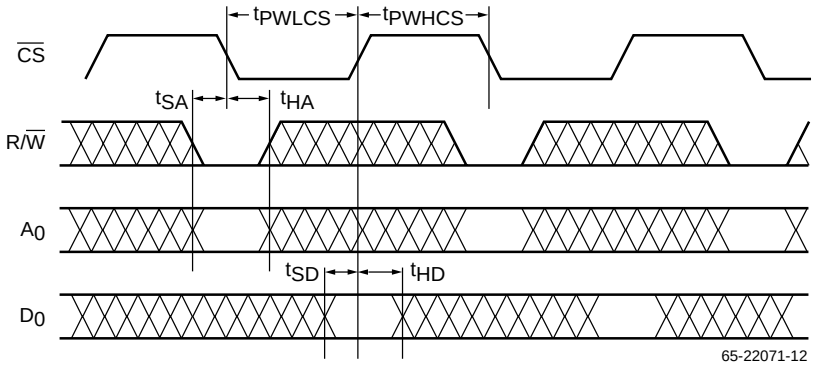


Figure 10. Microprocessor Port – Write Timing

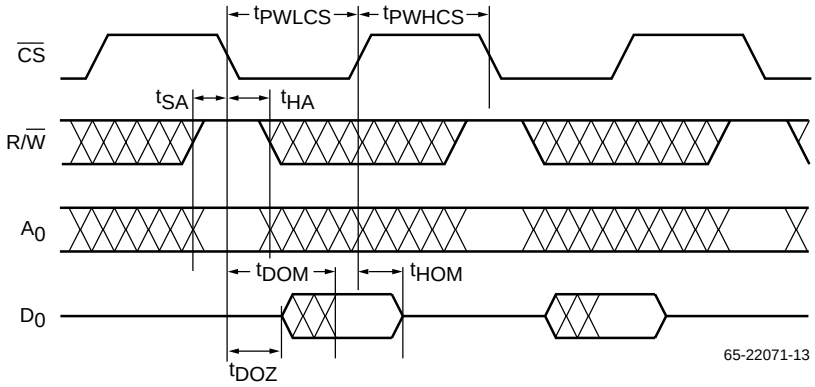


Figure 11. Microprocessor Port – Read Timing

Equivalent Circuits and Transition Levels

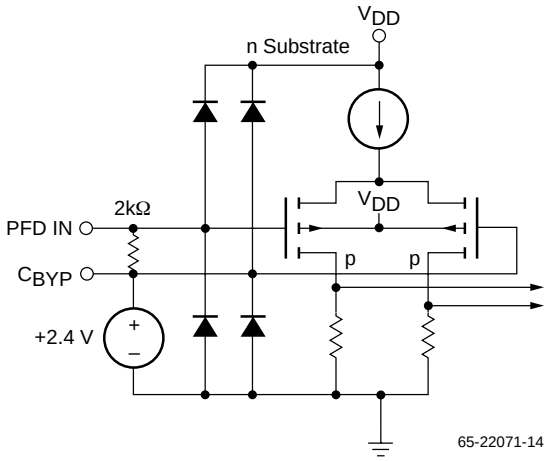


Figure 12. Equivalent PFD IN Circuit

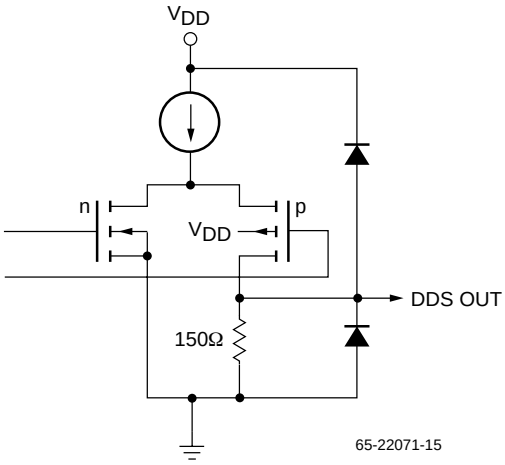


Figure 13. Equivalent DDS OUT Circuit

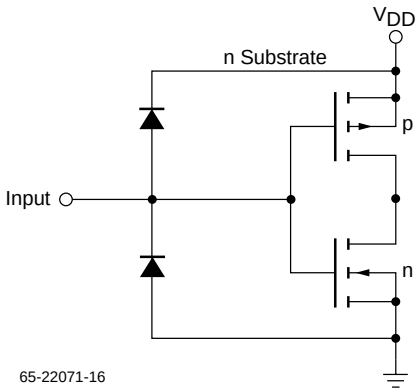


Figure 14. Equivalent Digital Input Circuit

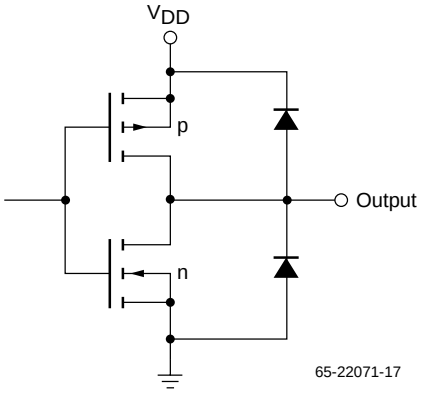


Figure 15. Equivalent Digital Output Circuit

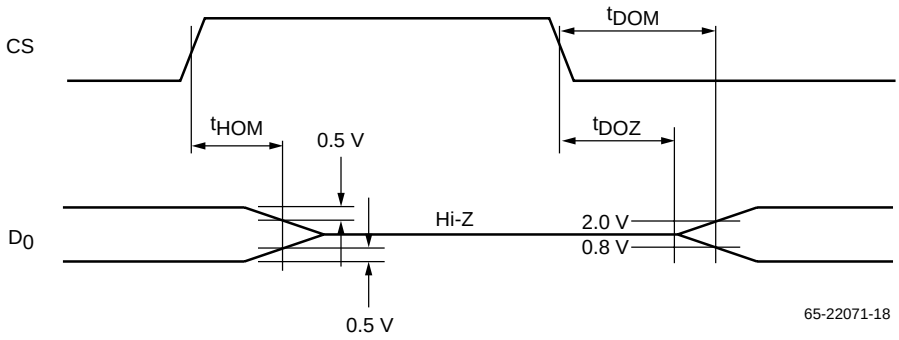


Figure 16. Transition Levels for Three-State Measurements

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min.	Max.	Unit.
Power Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	V_{DD} + 0.5	V
Digital Outputs			
Applied Voltage[2]	-0.5	V_{DD} + 0.5	V
Forced Current[3,4]	-6.0	6.0	mA
Short Circuit Duration (single output in HIGH state to GND)		1	sec
Temperature			
Operating, Case	-60	130	°C
Operating, Junction		150	°C
Lead Soldering (10 seconds)		300	°C
Vapor Phase Soldering (1 minute)		220	°C
Storage	-65	150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions (for standard temperature range)

Parameter		Min.	Nom.	Max.	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Inputs	2.0		V_{DD}	V
	CMOS Inputs	2/3V_{DD}		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				
	TTL Inputs	D_{GND}		0.8	V
	CMOS Inputs	D_{GND}		1/3 V_{DD}	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
V_{IN}	Video Input Signal Level, Sync Tip to Peak White		1.0		V
V_{REF}	External Reference Voltage		1.235		V
T_A	Ambient Temperature, Still Air	0		70	°C
Microprocessor Interface					
t_{PWHCS}	$\overline{CS}$ Pulse Width, LOW		50		ns
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH		50		ns
t_{SA}	Address Setup Time	0			ns
t_{HA}	Address Hold Time	16			ns
t_{SD}	Data Setup Time	20			ns
t_{HD}	Data Hold Time	0			ns

Note:

1. Timing reference points are at the 50% level.

Electrical Characteristics (for standard temperature range)

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current[1]	Total Current V_{DD} = Max, f_{PXCK} = 30MHz		190	230	mA
I_{REF}	Reference Inputcurrent	V_{REF} = +1.235V			100	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = 4.0V			±10	μA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0.4V			±10	μA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = -2.0 mA	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = 4.0 mA			0.4	V
I_{OZH}	Hi-Z Output Leakage current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	μA
I_{OZL}	Hi-Z Output Leakage current, LOW	V_{DD} = Max, V_{IN} =GND			±10	μA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1 Mhz		4	15	pF
C_O	Digital Output Capacitance	T_A - 25°C, f = 1 Mhz		10		pF
C_V	Input Capacitance, V_{IN1-3}	T_A = 25°C, f = 3.58 Mhz			15	pF
R_V	Input Resistance, V_{IN1-3}		50			kΩ

Note:

1. Typical I_{DD} with V_{DD} = +5.0 Volts and T_A = 25°C, Maximum I_{DD} with V_{DD} = +5.25 Volts and T_A = 0°C.

Switching Characteristics (for standard temperature range)

Parameter		Conditlons	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 35 pF	2		15	ns
t_{HO}	Output Hold Time		3		8	ns
f_{PCK}	Pixel Rate		12		15.3	MHz
f_{PXCK}	Master Clock Rate		24		30.6	MHz
t_{PWHPX}	PXCK Pulse Width, LOW		12			ns
t_{PWHPX}	PXCK Pulse Width, HIGH		12			ns
t_{DH}	Horizontal Sync to $\overline{GHSYNC}$			14		pixels
t_{VD}	Vertical Sync to $\overline{GVSYNC}$			14		pixels
t_{XL}	PXCK LOW to LDV HIGH				8	ns
t_{XV}	PXCK LOW to LDV LOW				8	ns
t_{DOM}	D_0 enable time			20		ns
t_{HOM}	D_0 disable time		10	15		ns
t_{DOZ}	$\overline{CS}$ LOW to D_0 output driven			5		ns

System Performance Characterlstics

Parameter		Min	Type	Max	Units
E_{SCH}	Sync time-base variation[1]			±3	ns
E_{SCP}	Subcarrier Phase Error[1]			±2	degrees
t_{AL}	Line-lock Acquisition Time			2	frames
V_{XT}	Channel-to-Channel Crosstalk @3.58 Mhz			-35	dB

Note:

1. NTSC/PAL compliant black burst at nominal input level ±10%, frequencies nominal ±10 ppm.

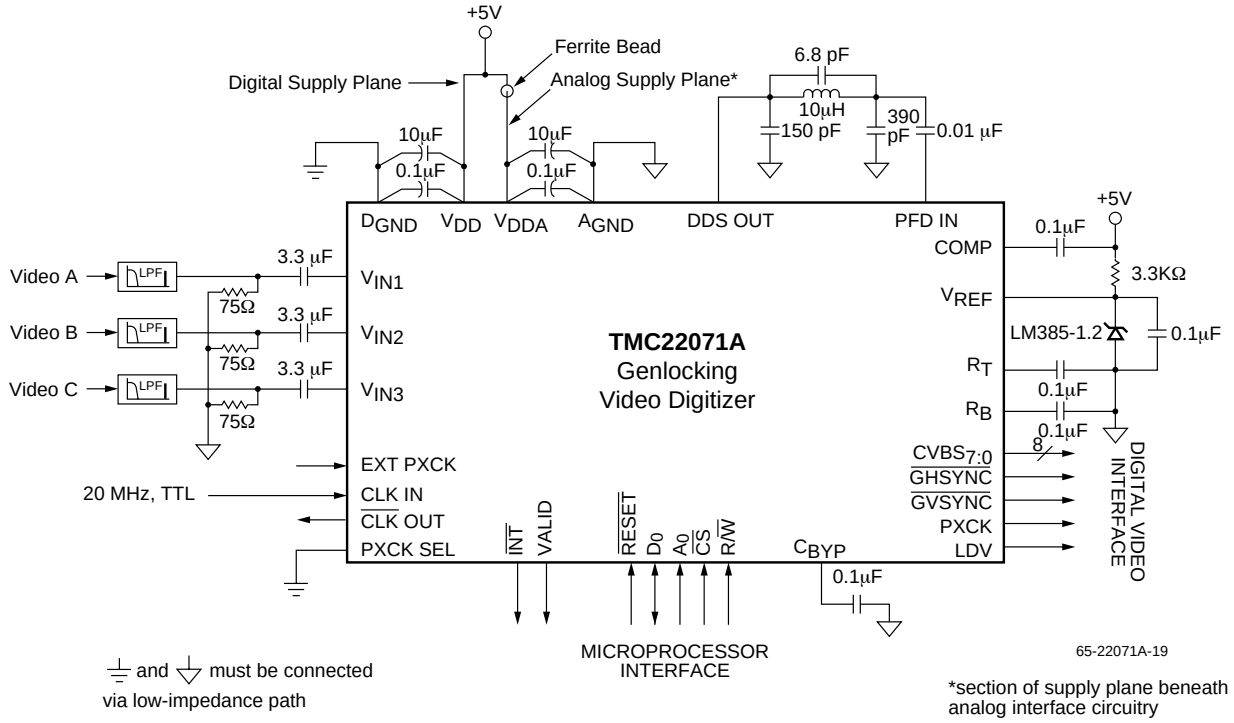


Figure 17. Typical Interface Circuit

Application Notes

The TMC22071A is a complex mixed-signal VLSI circuit. It produces CMOS digital signals at clock rates of up to 15 MHz while processing analog video inputs with a resolution of less than a few millivolts. To maximize performance it is important to provide an electrically quiet operating environment. The circuit shown in Figure 17 provides an optional external 1.2V reference to the V_{REF} input of the TMC22071A. The internal V_{REF} source is adequate for most applications.

FIltering

Inexpensive low-pass anti-aliasing filters are shown in Figures 18 and 20. These filters would normally be inserted in the video signal path just before the 75Ω terminating resistor and AC-coupling capacitor for each of the three video inputs, V_{IN1-3}. The filter of Figure 18 exhibits a 5th-order Chebyshev response with-3dB bandwidth of 6.7MHz and a group delay of 140 nanoseconds at 5MHz. The filter of Figure 19 has been equalized for group delay in the video signal band. Its -3dB passband is 5.5MHz while the group delay is constant at 220 nanoseconds through the DC to 5MHz frequency band.

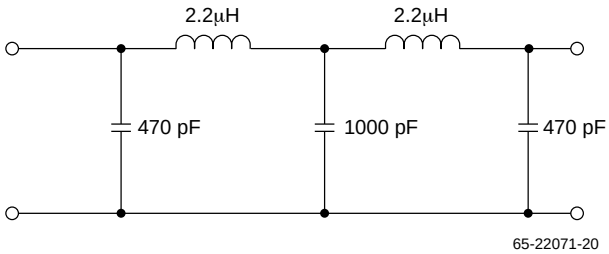


Figure 18. Simple Anti-aliasing Filter

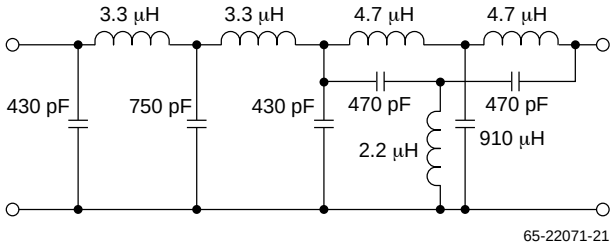


Figure 19. Group Delay Equalizer Filter

Using a 20 MHz Crystal

In systems where a 20 MHz clock is not available, a crystal may be used to generate the clock to the TMC22071A. The crystal must be a 20 MHz "fundamental" type, not overtone. Specific crystal characteristics are listed in Table 4 and the connections are shown in Figure 20.

Table 4. Crystal Parameters

Parameter	Value
Fundamental frequency	20 MHz
Tolerance	±30 ppm @ 25°C
Stability	±50 ppm, 0°C to 70°C
Load Capacitance	20 pF
Shunt Capacitance	7 pF Max.
ESR	50 Ω, Max.

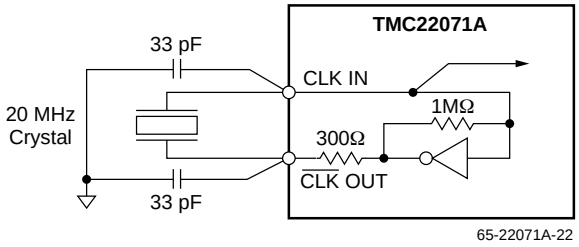


Figure 20. Direct Crystal Connections

Grounding

The TMC22071A has separate analog and digital circuits. To minimize digital crosstalk into the analog signals, the power supplies and ground connections are provided over separate pins (V_{DD} and V_{DDA} are digital and analog power supply pins; D_{GND} and A_{GND} are digital and analog ground pins). In general, the best results are obtained by tying all grounds to a solid, low-impedance ground plane. Power supply pins should be individually decoupled at the pin. Power supply noise isolation should be provided between analog and digital supplies via a ferrite bead inductor on the analog lead. Ultimately all +5 Volt power to the TMC22071A should come from the same power source.

Another approach calls for separating analog and digital ground. While some systems may benefit from this strategy, analog and digital grounds must be kept within 0.1V of each other at all times.

Interface to the TMC22x9x Encoder

The TMC22x9x Digital Video Encoders have been designed to directly interface to the TMC22071A Digital Video Genlock. The TMC22071A is the source for TMC22x9x input signals $CVBS_{7-0}$, $\overline{GHSYNC}$, $\overline{GVSYNC}$, LDV, and PXCK as shown in Figure 21. These signals directly connect to the TMC22x9x. The microprocessor interface for TMC22x9x and TMC22071A are identical. All R/$\overline{W}$, $\overline{RESET}$, data and address bus signals from the host microprocessor are shared by the TMC22x9x and TMC22071A. Only $\overline{CS}$, VALID, and $\overline{INT}$ signals are separate from the microprocessor bus.

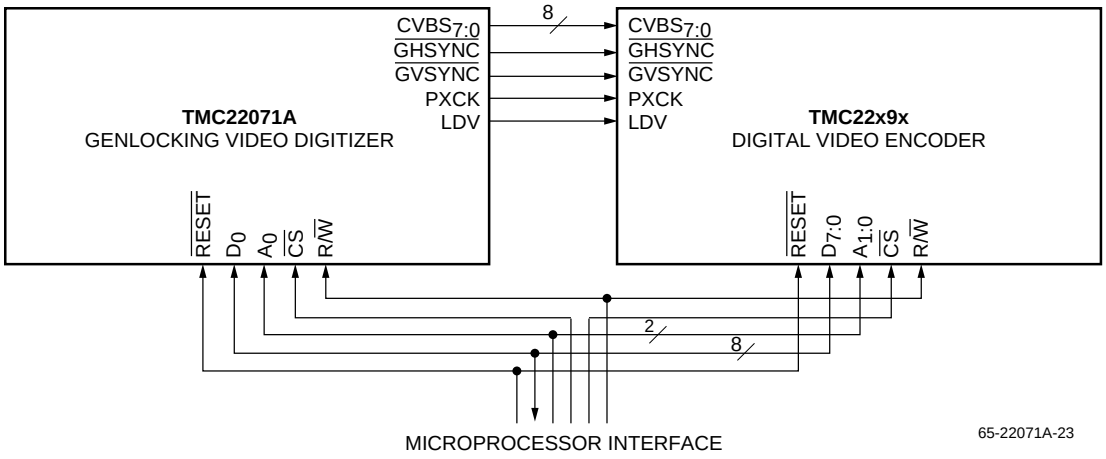


Figure 21. TMC22x9x Interface Circuit

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor picture quality. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (COMP,V_{REF}, R_T, R_B, DDS OUT, PFD IN, C_{BYP}, and V_{IN1-3}) as short as possible and as far as possible from all digital signals. The TMC22071A should be located near the board edge, close to the analog output connectors.

2. The digital power plane for the TMC22071A should be that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the analog power supply for the TMC22071A is the same as that of the system's digital circuitry, power to the TMC22071A V_{DDA} pins should be decoupled with ferrite beads and 0.1 μF capacitors to reduce noise.

3. The ground plane should be solid, nor cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They typically supply adjacent circuits on the device, which generate varying amounts of noise. For best results, use 0.1μF capacitors in parallel with 10μF capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC22071A, the voltage reference or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC22071A and its related analog circuitry can degrade performance.

6. CLK should be handled carefully. Jitter and noise on this clock or its ground reference may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Related Products

- TMC22x9x Digital Video Encoders
- TMC2242/TMC2243/TMC2246 Video Filters
- TMC2081 Digital Video Mixer
- TMC22x5y Digital Decoders
- TMC2302 Image Manipulation Sequencer

Notes:

Notes:

Notes:

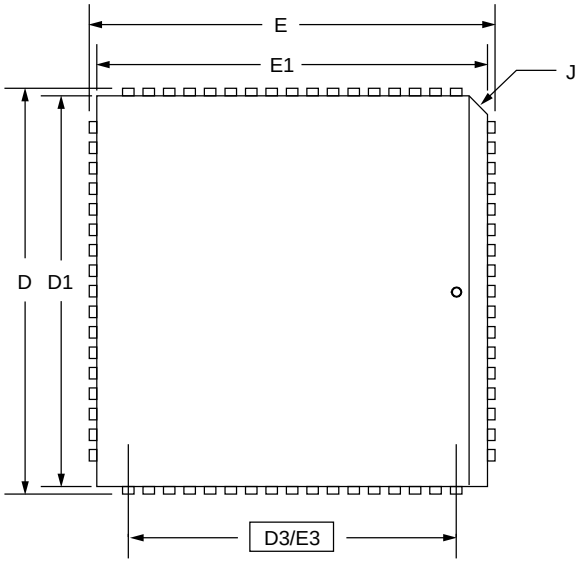
Mechanical Dimensions

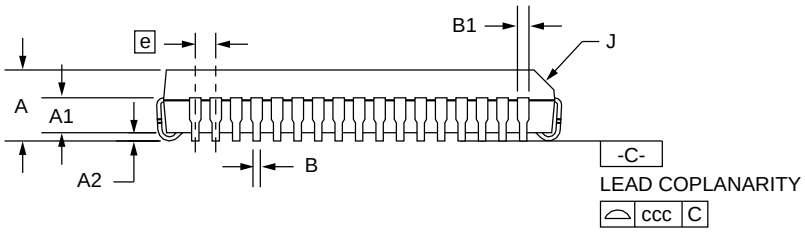
68 Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.200	4.19	5.08	
A1	.090	.130	2.29	3.30	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.985	.995	25.02	25.27	
D1/E1	.950	.958	24.13	24.33	3
D3/E3	.800 BSC		20.32 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	17		17		
N	68		68		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)





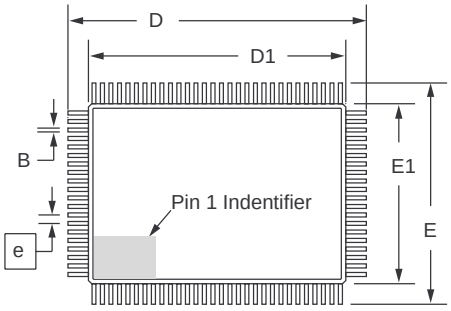
Mechanical Dimensions (continued)

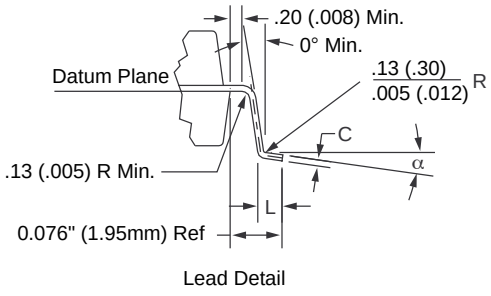
100 Lead MQFP Package – 3.2mm Footprint

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.008	.015	.22	.38	3, 5
C	.005	.009	.13	.23	5
D	.904	.923	22.95	23.45	
D1	.783	.791	19.90	20.10	
E	.667	.687	16.95	17.45	
E1	.547	.555	13.90	14.10	
e	.0256 BSC		.65 BSC		
L	.028	.040	.73	1.03	4
N	100		100		
ND	30		30		
NE	20		20		
α	0°	7°	0°	7°	
ccc	—	.004	—	.12	

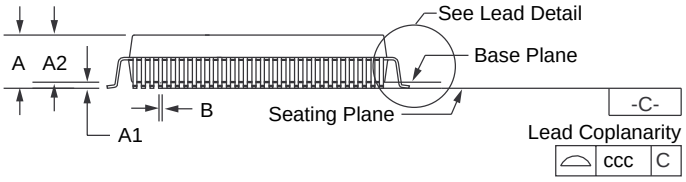
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC22071AR1C	T_A = 0°C to 70°C	Commercial	68-Lead PLCC	22071AR1C
TMC22071AKHC[1]	T_A = 0°C to 70°C	Commercial	100-Lead MQFP	22071AKHC

Note:

1. 100 Lead MQFP is strongly recommended for all new board designs.

7/24/98 0.0m 002
Stock#DS7022071A